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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM 10087416	FILING DATE 02/27/2002	CLASS 257	SUBCLASS 1.01	GAU 2811	EXAMINER OWENS
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**APPLICANTS: Trivedi Jigish; Wang Zhongze; Yang Rongsheng;

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A CON OF 09/444,024 11/19/1999
WHICH IS A DIV OF 09/386,076 08/30/1999 PAT 6,093,661

** FOREIGN APPLICATIONS VERIFIED:

NOTE: DISCLAIMER:
The term of this patent shall not extend
beyond the expiration date
of Pat. No. 6,417,546

PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO MI22-1965
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no	
Verified and Acknowledged Examiner's initials	
TITLE : Integrated circuitry and semiconductor processing method of forming field effect transistors	
U.S. DEPT. OF COMMERCE, PAT. & TRADEMARK OFFICE (Rev. 12-94)	

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED		
		Assistant Examiner	Total Claims	
			Print Claim for O.G.	
ISSUE FEE		Primary Examiner	DRAWING	
Amount Due	Date Paid		Sheets Drwg.	Figs. Drwg.
<input checked="" type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner	
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